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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,946	10/21/2003	Robert H. Bishop	5646-98	4031

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,946	BISHOP ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-10,12-16,18-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-10,12-16,18-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable Iwasaki (US Pat. 5814890) in view of Melton et al. (US Pat. 5269453).

Regarding claims 8-10, Iwasaki discloses a grid array microelectronic package (GAP) comprising:

- a circuit board substrate/first substrate (CBS-7 in Fig. 3-5)
- an array/first array of external connectors (10 in Fig. 3-5) on the substrate that are arranged in a plurality of rows and columns to define a periphery of the array along outer two rows and two columns towards edges of the CBS and an interior of the array, the external connectors being in a form of flat pad/bump (see 10 in Fig. 3)
- the array further including a variety of configurations of the external connectors having five rows and eleven columns (see Fig. 7-13), including a pair of peripheral rows and a pair of peripheral columns at a periphery thereof and pairs

of interior rows and interior columns between the respective pair of peripheral rows and peripheral columns, wherein an external connector in the peripheral column and one external connector in an interior column adjacent thereto are missing (see two or more missing connectors from the peripheral columns in the configurations of Fig. 7-13) from the array to define a routing channel that extends from the periphery of the array towards the interior of the array, and

- the configuration comprising the arrays including 25 missing connectors (see Fig. 6), 31 missing connectors (see Fig. 7), etc.

(Fig. 3-13; Col. 4, line 65- Col. 7, line 58).

Iwasaki fails to teach a plurality of signal conductors that extend from outside the array of external connectors along the routing channel and electrically connect to a plurality of the external connectors in an interior row or interior column adjacent the routing channel.

Melton et al. teach a grid array package (see Fig. 1-3) having a printed circuit board (PCB-12 in Fig. 1) substrate where a plurality of electrical traces/runners/signal conductors (see 24/20 in Fig. 1-3) along the routing section/channel on the PCB are used to provide the desired electrical connection to respective external connectors (see 30 in Fig. 1-3) in an interior section of an array having external connectors (Col. 2, line 55- Col. 5, line 2).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the a plurality of signal conductors that extend from outside the array of external connectors along the routing channel and electrically connect to a plurality of the external connectors in an interior row or interior column adjacent the routing channel as taught by Melton et al. so that the desired routing for the external connectors can be achieved in Iwasaki's GAP

3. Claims 12-16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki (US Pat. 5814890) and Melton et al. (US Pat. 5269453) as applied to claims 8-10 above, and further in view of Dockerty et al. (US Pat. 5796169).

Regarding claims 12 and 13, Iwasaki teaches substantially the entire claimed structure as applied to claims 8-10 above, except the package further comprising:

- a second substrate, and
- a second array of external connectors on the second substrate that are arranged to mate with the first array of external connectors.

Dockerty et al. teach a ball grid array (BGA) package having a first substrate (see printed circuit board 1 in Fig. 1 and 2) and a second substrate (see an integrated circuit device 3 in Fig. 1 and 2) having respective first and second arrays comprising external solder ball/bump connectors (see 11 in Fig. 1-3) where the second array of external

connectors on the second substrate are bonded/mated with the respective first array of external connectors to provide the desired interconnection (Fig. 1-3; Col. 3 and 4)

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second substrate and the second array of external connectors on the second substrate being arranged to mate with the first array of external connectors as taught by Dockerty et al. so that the desired interconnection and circuit routing between the two substrates can be achieved in Iwasaki's GAP.

Regarding claims 14-16, Iwasaki and Melton et al. teach substantially the entire claimed structure as applied to claim 8 above, except at least one external connector in a peripheral row or peripheral column and at least one external connector in an interior row or interior column adjacent thereto are electrically strapped together to define a routing channel that extends from the periphery of the array towards the interior of the array.

Dockerty et al. teach the BGA package having the external solder ball/bump connectors (see SBC 11 in Fig. 1-4) where the SBC are electrically connected/strapped in a variety of connecting patterns having support solder (see 16, 17, 18, 23, etc. in Fig. 3) to provide the desired electrical and thermal conduction (Col. 4, line 35- Col. 5, line 25), such patterns defining the routing channels including those that extend from the periphery of the array towards the interior of the array including two or more

bumps/external connectors (see the pattern 23 in the farthest right in the region 22 extending from the right peripheral column into the interior row/column in Fig. 3).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one external connector in a peripheral row or peripheral column and at least one external connector in an interior row or interior column adjacent thereto are electrically strapped together to define a routing channel that extends from the periphery of the array towards the interior of the array as taught by Dockerty et al. so that the desired electrical/thermal conduction and circuit routing can be achieved in Melton et al. and Iwasaki's GAP.

Regarding claims 18 and 19, Iwasaki, Melton et al. and Dockerty et al. teach substantially the entire claimed structure as applied to claims 8 and 12-14 above.

4. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki (US Pat. 5814890) and Melton et al. (US Pat. 5269453) to claims 8-10 above, and further in view of Kimura et al. (US Pat. 6677677).

Regarding claims 20-22, Iwasaki and Melton et al. teach the entire claimed structure as applied to claims 8-10 above, except at least one external connector in a peripheral row or column and at least one external connector in an interior row or column adjacent

thereto are operationally disconnected from the substrate to define a routing channel that extends from the periphery of the array towards the interior of the array.

Kimura et al. teach a GAP having external dummy bumps/external connectors and external functional bumps/external connectors (see 3 and 2 respectively in Fig. 1) where the bump/external connector in a peripheral row and at least one external connector in an interior row adjacent thereto is dummy/operationally disconnected from the substrate (see the array of 3 in the bottom row and the adjacent row in the third column from right in Fig. 1) to define a routing channel that extends from the periphery of the array towards the interior of the array. Furthermore, such routing channels can include two or more adjacent dummy/operationally disconnected bumps/external connectors in the area having missing connectors in the peripheral row and the adjacent interior rows and extending from the periphery of the array towards the interior of the array (see the array of 3 in the third column from right in Fig. 1; Col. 2, lines 30-58).

5. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki (US Pat. 5814890), Melton et al. (US Pat. 5269453) as applied to claim 20 above, and further in view of Kimura et al. (US Pat. 6677677) and Dockerty et al. (US Pat. 5796169).

Regarding claims 24 and 25, Iwasaki, Melton et al., Kimura et al. and Dockerty et al. teach substantially the entire claimed structure as applied to claims 8, 12, 13 and 20 above.

Response to Arguments

6. Applicant's arguments with respect to claims 8-10, 12-16, 18-22, 24 and 25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

02-23-05

NITIN PAREKH

PRIMARY EXAMINER

Technology Center 2800